

# Multi-beam 4 GHz Microwave Apertures Using Current-Mode DFT Approximation on 65 nm CMOS

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## Abstract

A current-mode CMOS design is proposed for realizing receive mode multi-beams in the analog domain using a novel DFT approximation. High-bandwidth CMOS RF transistors are employed in low-voltage current mirrors to achieve bandwidths exceeding 4 GHz with good beam fidelity. Current mirrors realize the coefficients of the considered DFT approximation, which take simple values in  $\{0, \pm 1, \pm 2\}$  only. This allows high bandwidths realizations using simple circuitry without needing phase-shifters or delays. The proposed design is used as a method to efficiently achieve spatial discrete Fourier transform operation across a ULA to obtain multiple simultaneous RF beams. An example using 1.2 V current-mode approximate DFT on 65 nm CMOS, with BSIM4 models from the RF kit, show potential operation up to 4 GHz with eight independent aperture beams.

## Keywords

Analog, arrays, beamforming, aperture, multibeam.

## 1 INTRODUCTION

The formation of multiple orthogonal radio-frequency (RF) beams are a quintessential example of antenna arrays [1, 2]. There are applications for multi-beam arrays, such as wireless communications, radar, radio astronomy, and space imaging. Alternative to phased-arrays [3] that achieve a single steerable beam, multiple simultaneous RF beams—directed at fixed directions—are achieved

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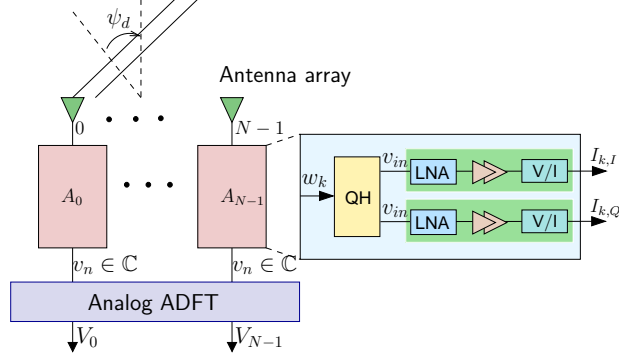


Figure 1: Analog RF 8-beam aperture using a spatial 8-point DFT approximation.

using a *spatial discrete Fourier transform (DFT) operation* across a uniformly-spaced array [4, 5]. In digital radar, multi-beams are achieved by digitizing the intermediate frequency (IF) signals from each element receiver, which are connected to the array. Sampling is followed by an application of the  $N$ -point spatial DFT computed via a fast Fourier transform (FFT) on a per-frame basis [4, 5].

The use of an 8-point approximate DFT, implemented by means of a fast algorithm [6], where DFT-beams have been closely emulated using a matrix of Gaussian integer weights, allows multi-beams using relatively simple active RF circuits. Approximate transformations are linear transformations of low computational cost offering close results to that from the exact transformation. The realization of multi-beams in analog by mean of a DFT approximation using microwave circuits exploits the high-bandwidth of current-mode CMOS integrated circuits. The approximate DFT achieves RF beams that are nearly identical to DFT-beams albeit without a Butler Matrix. That is, the analog circuit becomes quite simple to design owing to the use of current mirrors having weights over the set  $\mathcal{P} = \{0, \pm 1, \pm 2\}$  only. We show that such an approximation can be efficiently realized at 4 GHz or more of bandwidth using analog IC designs. Fig. 1 shows the overview of the aperture array, where  $N$  elements makeup a uniformly-spaced linear array (ULA) with spacing  $\Delta x$ . The elements (e.g., Vivaldi or spiral antennas) are amplified and quadrature down-converted or fed through a quadrature hybrid (QH) to achieve complex inputs for the 8-point DFT approximation.

## 2 8-POINT APPROXIMATE DFT MULTI-BEAM MATRIX

Recall that a DFT is a discrete orthogonal transformation that transforms an input vector  $\mathbf{v} = [v_0(t) \ v_1(t) \ \cdots \ v_N(t)]^\top$  to an output vector with  $N$  spectral coefficients, denoted by  $\mathbf{V} = [V_0(t) \ V_1(t) \ \cdots \ V_N(t)]^\top$  [7], each corresponding to a far-field RF beam for  $N$  element arrays when  $v_k(t) = x_I(t) + jx_Q(t) \in \mathbb{C}$  consist of in-phase ( $x_I(t)$ ) and quadrature ( $x_Q(t)$ ) antenna feeds from a QH component per array element, and where  $V_k(t) = \sum_{n=0}^{N-1} v_n(t) \cdot \omega_N^{kn}$ ,  $k = 0, 1, \dots, N-1$ , where  $j = \sqrt{-1}$  and  $\omega_N = \exp\left\{-\frac{2\pi j}{N}\right\}$  is the  $N$ th root of unity. In matrix form,  $\mathbf{V} = \mathbf{F}_N \cdot \mathbf{v}$  and

$\mathbf{v} = \mathbf{F}_N^{-1} \cdot \mathbf{V} = \frac{1}{N} \cdot \mathbf{F}_N^* \cdot \mathbf{V}$ , where  $\mathbf{F}_N$  is the DFT transformation matrix whose  $(i, k)$ th element is  $f_{i,k} = \omega_N^{(i-1)(k-1)}$ , for  $i, k = 1, 2, \dots, N$  and the superscript  $*$  denotes the transposed conjugation (Hermitian). Classical radar apertures obtain multi-beams using a Butler Matrix realization of the DFT. For the derivation of DFT approximations, we consider the set  $\mathcal{Q} = \left\{ z \in \mathbb{C} : \Re\{z\} \in \mathcal{P} \wedge \Im\{z\} \in \mathcal{P} \right\}$  for the matrix entries of the DFT approximation matrices. Parametric optimization, which minimizes the Frobenius norm, over the set  $\mathcal{Q}$  leads to an 8-point DFT approximation having near-orthogonality and low circuit complexity. The optimal elements for the parametric approximation of  $\mathbf{F}_8$  are 1,  $(1-j)/2$ , and  $-j$ . Thus, the resulting approximate DFT matrix contains only Gaussian integer entries:

$$\hat{\mathbf{F}}_8 = \frac{1}{2} \cdot \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ 2 & 1-j & -2j & -1-j & -2 & -1+j & 2j & 1+j \\ 2 & -2j & -2 & 2j & 2 & -2j & -2 & 2j \\ 2 & -1-j & 2j & 1-j & -2 & 1+j & -2j & -1+j \\ 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ 2 & -1+j & -2j & 1+j & -2 & 1-j & 2j & -1-j \\ 2 & 2j & -2 & -2j & 2 & 2j & -2 & -2j \\ 2 & 1+j & 2j & -1+j & -2 & -1-j & -2j & 1-j \end{bmatrix}.$$

The above 8-point approximate DFT matrix  $\hat{\mathbf{F}}_8$  preserves the symmetry of the DFT and has null multiplicative complexity—a salient property that allows realization using current-mode circuits having integer multiplications of current values that map neatly into multiples of identical 1:1 mirrors on an analog IC. Let  $\mathbf{I}_n$  be the identity matrix of order  $n$  and  $\mathbf{B}_n = \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix} \otimes \mathbf{I}_{n/2}$ , where  $\otimes$  denotes the Kronecker product. Matrix factorization techniques leads to an algorithm for mapping to analog circuits [7]. In particular,  $\hat{\mathbf{F}}_8$  admits the following factorization:

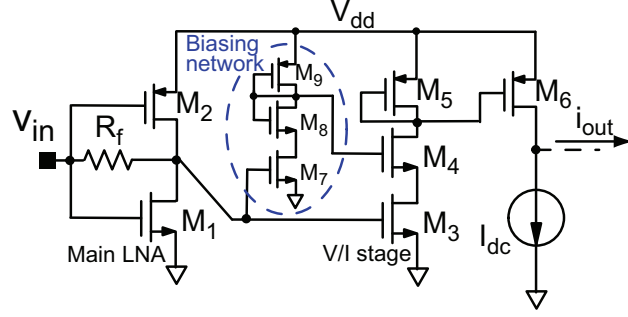
$$\begin{aligned} \hat{\mathbf{F}}_8 = & \mathbf{P} \times \text{diag}(\mathbf{I}_2, \mathbf{A}_1, \mathbf{A}_3) \times \mathbf{D}_2 \times \text{diag}(\mathbf{B}_2, \mathbf{I}_2, \mathbf{A}_4) \\ & \times \mathbf{D}_1 \times \text{diag}(\mathbf{B}_4, \mathbf{A}_2) \times \mathbf{B}_8, \end{aligned}$$

where  $\mathbf{A}_1 = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}$ ,  $\mathbf{A}_2 = \begin{bmatrix} 1 & & 1 \\ & 1 & -1 \\ 1 & & -1 \end{bmatrix}$ ,  $\mathbf{A}_3 = \begin{bmatrix} 1 & -1 & & 1 \\ & 1 & -1 & 1 \\ & & 1 & 1 \end{bmatrix}$ ,  $\mathbf{A}_4 = \begin{bmatrix} 1 & & & 1 \\ & 1 & -1 & \\ 1 & & -1 & \\ & & & -1 \end{bmatrix}$ ,  $\mathbf{D}_1 = \text{diag}(1, 1, 1, 1, 1, 1/2, 1, 1/2)$ ,  $\mathbf{D}_2 = \text{diag}(1, 1, 1, j, 1, j, j, 1)$ ,  $\mathbf{P} = [\mathbf{e}_1 | \mathbf{e}_5 | \mathbf{e}_3 | \mathbf{e}_6 | \mathbf{e}_2 | \mathbf{e}_8 | \mathbf{e}_4 | \mathbf{e}_7]^\top$  is a permutation matrix, and  $\mathbf{e}_i$  is the 8-point column vector with element 1 at the  $i$ th position and 0 elsewhere.

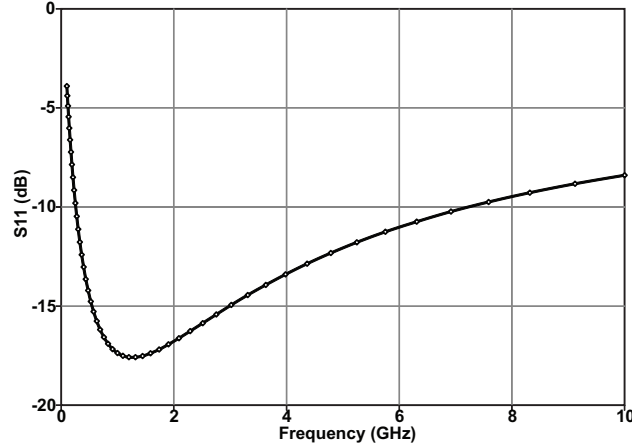
### 3 8-BEAM 4 GHz DFT APPROXIMATION IN 65 NM CMOS

#### 3.1 ANTENNA FRONT-END

A conventional inverter-based shunt feedback LNA, shown in Fig. 2(a), is employed. The input signal,  $v_{\text{in}}$ , from each antenna is applied to the gates of  $M_1$  and  $M_2$ , forming the main LNA, whose  $S_{11}$ , displayed in Fig. 2(b), is set with  $R_f$  and the transconductances of  $M_{1,2}$ . The cascoded transistors  $M_{3,4}$  are used to increase the impedance at the drain of  $M_5$  so that most of the small-



(a)



(b)

Figure 2: 65 nm 1.2 V CMOS LNA with current output  $i_{out}$  (top); amplifier  $|S_{11}|$  [dB] better than  $-10$  dB up to 7 GHz (bottom).

signal current flows into the  $M_{5,6}$  current mirror. The circuit consisting of  $M_{3-6}$  forms a voltage-to-current (V/I) conversion stage. A DC current source  $I_{dc}$  reduces the DC component of the  $i_{out}$  current. The gate bias for  $M_4$  is provided by a biasing network consisting of  $M_{7-9}$ , which are scaled versions of  $M_{3-5}$ . The LNA draws 26.25 mA from a 1.2 V DC supply.

### 3.2 CURRENT MODE ANALOG 8-POINT APPROXIMATE DFT

The matrix  $\hat{\mathbf{F}}_8$  is realized in current mode to increase operational bandwidth. The signals from each LNA+secondary amplifier at the antennas (Fig. 1) are converted to output currents  $i_{out}$ . Eight such small-signal current outputs form the input signals for the current-mode realization of the discussed 8-point approximate DFT. The real and imaginary components of the considered approximate DFT matrix are realized separately. Fig. 3(a) shows a NMOS current copier used to realize one column of the DFT approximation matrix (real part). Fig. 3(b) shows the PMOS based current subtractor needed for negative valued entries of the DFT approximation matrix. Example building blocks for the NMOS and PMOS current combiners in Fig. 3(a-b) are provided in Fig. 3(c-d), respectively.

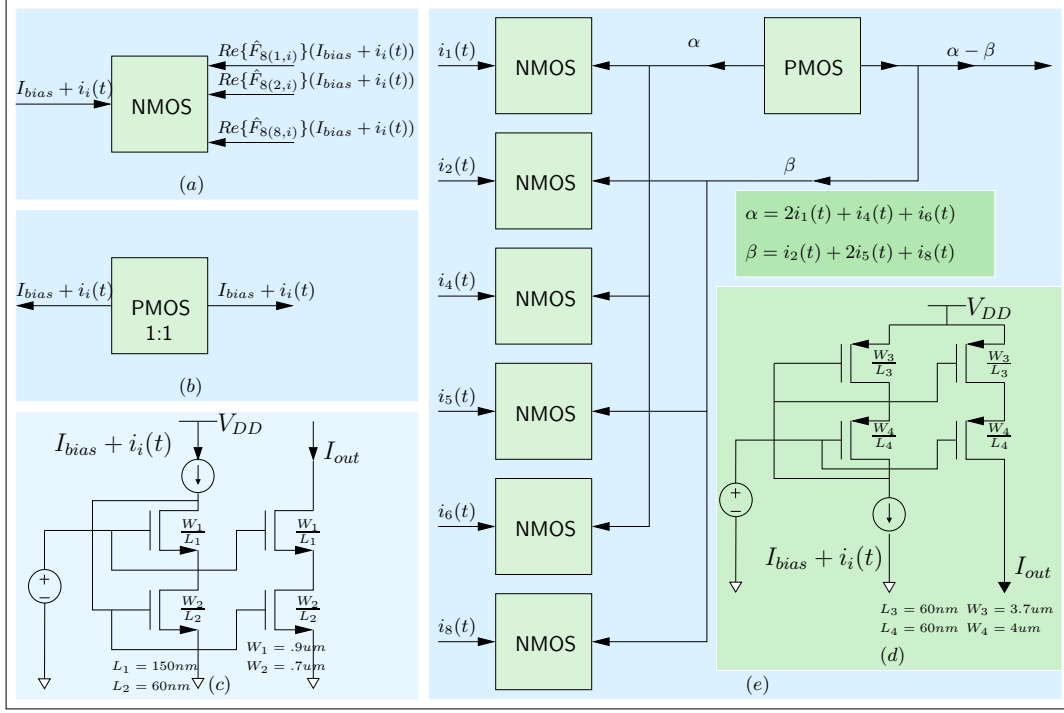


Figure 3: Current mode implementation of the 8-point DFT approximation using 65 nm CMOS RF NMOS/PMOS mirrors.

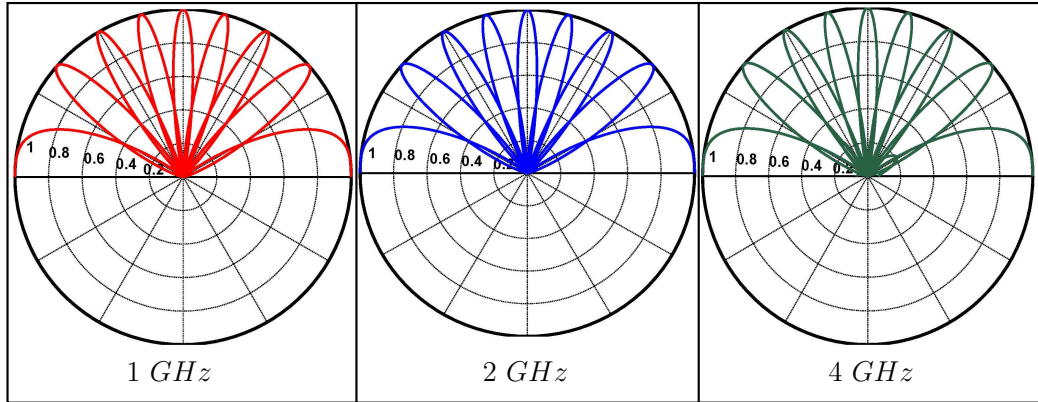


Figure 4: Polar response patterns for current outputs at 1, 2, and 4 GHz.

The DC bias current for the NMOS mirror in Fig. 3(c) is  $I_{\text{bias}} = 100 \mu\text{A}$ . An example of one row of the 8-point approximate DFT (row 4) is shown in Fig. 3(e). All signal currents are assumed to be small (1–10%) compared to DC bias currents. Each current mirror is designed using the low-voltage cascode topology [8]. The technology used is 65 nm GP CMOS, and all transistors are from the RF kit, with supply voltage 1.2 V. Simulations are in Cadence Spectre and employ BSIM4 RF transistor models.

### 3.3 BSIM4 ARRAY PATTERNS

The Cadence designs were simulated at frequencies  $f \in \{1, 2, 4\}$  GHz. The input currents were maintained at  $2\mu\text{A}$  peak-to-peak. The time-domain response was simulated, in steady state, and the peak-to-peak values were noted. The simulated small-signal output currents from the 8-point DFT approximation outputs were used to compute the polar response patterns for each current mode circuit for three frequencies in Fig. 4. The polar patterns obtained from the BSIM4 models of the discussed DFT approximation is very close to the expected ideal polar patterns linked to the theoretical 8-point DFT approximation. At higher frequencies, from the low-pass effects of the current mirrors due to dominant parasitic poles of the CMOS circuit, the pattern deviates noticeably (not shown here). The 8-point approximate DFT provides far-field receive beams at directions  $90.0^\circ$ ,  $48.5^\circ$ ,  $30.0^\circ$ ,  $14.5^\circ$ ,  $0.0^\circ$ ,  $-14.5^\circ$ ,  $-30.0^\circ$ , and  $-48.5^\circ$  measured from the array.

## 4 CONCLUSION

The discussed DFT approximation is a numerical efficient method for the approximate DFT evaluation, and requires only small Gaussian integer valued weights. A multi-beam aperture algorithm and analog RF CMOS implementation for the 8-point approximate DFT was proposed, designed, simulated and evaluated, for beamforming at bandwidths up to 4 GHz using ULAs of wideband elements. The analog approximate DFT circuit was designed using 65 nm GP CMOS employing RF transistors, with low-voltage current mirrors for maximum peak-peak swings and bandwidth. Cadence BSIM4 models verify the aperture provides eight RF beams up to 4 GHz when supplied with 1.2 V DC.

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